REMARKS

Several editorial changes have been made in the specification, claims and abstract.

Amendment in the specification has been made by way of a substitute specification pursuant to 37 C.F.R. §§ 1.121(b)(3) and 1.125(b). The amendments in the specification and abstract contain only editorial corrections and include no new matter. Entry of the substitute specification is respectfully requested.

The drawings have been amended to correct several clerical mistakes. In Fig. 1, the reference numeral 10 in the drawing as originally filed incorrectly points to the epitaxial layer 10. The reference numeral 10, which designates an insulating layer throughout the specification, should point to the insulating layer. In Fig. 3, a cut-line arrowhead with the number 4 was inadvertently left in Fig. 3 as originally filed and should be removed. Applicant submits herewith annotated sheets showing changes and replacements sheets incorporating the aforementioned change in the Appendix after page 14. Approval and acceptance of the replacement drawings as substitutes for the original drawings as filed are respectfully requested.

Claim 13 was rejected under 35 U.S.C. § 112, second paragraph, as having insufficient antecedent basis. By this amendment, claim 13 has been amended. The definite article "said" before "low resistance trenches" has been deleted, thereby obviating the Examiner's rejection. Withdrawal of the rejection on claim 13 is hereby respectfully requested.

Claim 1 was rejected under 35 U.S.C. § 102(e) as being anticipated by *Uenishi et al.* (U.S. Patent No. 5,894,149).

Applicant respectfully submits that Claim 1 as originally filed defines over *Uenishi et al.* Specifically, claim 1 recites, *inter alia*, "a first insulating layer disposed on said major surface above said trench, said first insulating layer having a first contact opening." The structure of *Uenishi et al.* does not have a "first insulating layer having a first contact opening." Referring to Fig. 1 in conjunction with the description on column 11 lines 39-42 of *Uenishi et al.*, the layer 7 is described as an insulating film which is arranged to encompass the gate electrode 8. There is no opening formed in the insulating film 7 of *Uenishi et al.* for purpose of allowing the material inside the trench 70 to make contact with another material. For the sake of argument, assume the transformation section of the trench 70 from the narrower section to the wider section is an "opening." The "opening" surely is not for the purpose of "contacting." That is, as commonly understood in the art and is so claimed in applicant's claim 1, a contacting opening is an void which is formed for the purpose of allowing material thereunder to make contact with yet another material disposed thereabove. In *Uenishi et al.*, the material 8a encompassed by

the insulating film 7 is homogenous made of polysilicon (Figs. 17, and column 15, lines 9-11 of *Uenishi et al.*). The "opening" in *Uenishi et al.* is not and should not be construed as a "contact opening."

To further distinguish over *Uenishi et al.*, claim 1 has been amended. Amended claim 1 now recites, in addition to above, "said first conductive layer having conductivity higher than the conductivity of said conductive material." The structure of *Uenishi et al.* does not have such a first layer with conductivity higher than the conductivity of the conductive material deposited inside the trench. As said before, the gate electrode 8 of *Uenishi et al.* is made of polysilicon homogeneously disposed in the insulating film 7. Again, for purpose of argument, if strainedly construing the wider portion of the gate electrode 8 as a first conducting layer and the narrower portion as the conductive material, then the conductivities of the two portions are the same and not arranged as having "said first conductive layer having conductivity higher than the conductivity of said conductive material," as recited in Applicant's amended claim 1. Accordingly, amended claim 1 is not anticipated by *Uenishi et al.* and withdrawal of the rejection is respectfully requested.

Applicant further submits that claim 1 is nonobvious in light of the prior art. In a trench MOSFET (Metal Oxide Semiconductor Field Effect Transistor) structure having trench gates, the trench gates are normally tied together. In most prior art trench MOSET devices, the polysilicon in the trench gates are electrically connected together by no other material but polysilicon itself. Polysilicon is a short name for polycrystalline silicon, which as the name implies, does not have an uniform crystallized structure but instead with numerous crushed particles of silicon. Each silicon particle has a crystal structure of its own. When properly doped with impurities, polysilicon can be conductive. Yet the conductivity is inferior to that of some other conductive materials, such as metal or alloy. This is so stated in Applicant's disclosure on page 4, lines 6-8 (¶ [0009] in the substitute specification). In connecting the gates of the MOSFET cells, merely linking polysilicon in the trench gates with polysilicon does not have the performance advantage as Applicant's claimed invention in several aspects.

The first aspect relates to the static or DC (direct current) performance. That is, there are no switchings or varying signals applied to the MOSFET during operation. As mentioned earlier, polysilicon has a relatively low conductivity. To compensate for the relatively low conductivity, in contacting the polysilicon gates of a MOSFET array, as shown in Applicant's disclosure in Fig. 2 and the accompanying description on page 3, lines 1-14 (¶ [0006] of the substitute specification), protruding fingers 22A distributed throughout the array are commonly laid out. This is especially true with a MOSFET device having a large number of array cells in which multiple fingers, such as protruding fingers 22A are incorporated. The arrangement is analogous to mid-tapping a high-resistance discrete resistor to curtail resistance. To accommodate the protruding gate metal fingers, the source metal layer 13 is also segmented and consequently the source

metal layer 13 itself is burdened with higher electrical resistance. Increase in resistance of the source metal layer 13 negatively impacts the all important parameter, the power-on resistance, R_{ON}. The reason is the power-on current of a MOSFET device flows through the thin cross-sectional area of the source metal layer 13. As is known in the art, the smaller the area for the current flow, the higher is the Ohmic resistance. Segmenting the source metal layer 13 surely decreases certain cross-sectional areas of the layer 13 in the form of current bottlenecks, and as a result increases the power-on resistance, R_{ON}. Modern-day MOSFET devices have the power-on resistance, R_{ON}, running in milliohm ranges. The detrimental effect to the power-on resistance parameter, R_{ON}, can be significant for a MOSFET device with a segmented source metal layer.

There is still yet another undesirable effect. To communicate with the outside world, the MOSFET device needs to be bond-wired into a chip carrier. Again, referring to Fig. 2 of Applicant's disclosure, for each bond wire bonding to the source metal layer 13, one end of the bond wire is shaped (e.g., by untrasound) in the form of a bead which in turn is soldered onto the source metal layer 13. If the source metal 13 is segmented as shown in Fig. 2 and the accompanying discussion in Applicant's disclosure on page 5, lines 14-25 (¶ [0012] of the substitute specification), the bonding beads at the terminals of the bond wires are confined to the restricted area 30. Wire-bonding of a MOSFET device under such restraint is more costly and prone to bond-wire misstepping and consequently increase the manufacturing costs.

However, the more important aspect concerns with the dynamic performance. Other than operating under a DC condition as aforementioned, a MOSFET device very often is used in a dynamic environment. For example, the MOSFET device may be a component of a switching power supply. In common practice, the power supply is switching at a high-frequency range. As such, the MOSFET device must be able to operate under high-frequency operations. In most prior art MOSFET devices, the trench gates are linked together by polysilicon. The relatively high resistivity of the polysilicon manifests itself as high distributed resistance along the gate-to-source input path of the entire MOSFET structure, thereby undermining the overall timing responses. Put another way, the relatively low conductivity of the linking polysilicon retards the RC (resistance-capacitance) time constant of the gate-to-source input path of the overall structure and renders the resultant MOSFET device incapable of operating in high-frequency applications. Again, this is all explained in Applicant's disclosure on page 4, lines 6-16 (¶ [0009] in the substitute specification).

If Applicant's invention were in fact obvious, because of its advantages as aforementioned, those skilled in the art surely would have implemented it by now. That is, the fact that those skilled in the art have not implemented the invention, despite its great advantages, indicates that it is not obvious.

For the reasons stated above, Applicant respectfully submits that claim 1 is neither anticipated nor rendered obvious by *Uenishi et al.* Withdrawal of the rejection on claim 1 under 35 U.S.C. § 102(e) is believed to be in order and is respectfully requested.

Claim 1-3 and 7 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Kubo et al.* (U.S. Patent No. 5,972,741).

For the same reasons as stated previously, Applicant submits that claims 1-3 and 7 are neither anticipated nor rendered obvious by *Kubo et al.*

Referring to Fig. 1 and the accompanying description on column 1, lines 25-27 of *Kubo et al.*, the polysilicon gate 4 is formed of having polysilicon deposited within an insulating film 3. In a manner similar to *Uenishi et al.* as discussed earlier, the structure of *Kubo et al.* does not have any opening for purpose of contacting different materials, and further without "said first conductive layer having conductivity higher than the conductivity of said conductive material," in which the conductive material is deposited inside the gate trench as recited in Applicant's amended claim 1. Likewise, in a manner similar to *Uenishi et al.*, the MOSFET device of *Kubo et al.* does not have the static and dynamic performances as claimed in Applicant's invention, also as discussed earlier.

Claims 2, 3 and 7 are dependent claims dependent upon claim 1 and with all the limitations of claim 1, are submitted to be patentable for the same reason claim 1 is believed to be patentable. Accordingly, Applicant respectfully requests withdrawal of claims 1-3 and 7 under 35 U.S.C. § 102(e) as being anticipated by *Kubo et al.*

Claims 1-12, 14-19 and 21-31 furthermore were rejected under 35 U.S.C. § 103 (a) as being unpatentable over *Uenishi et al.* or *Kubo et al.* in view of *Blanchard* (U.S. Patent No. 5,034,785). In the rejection, the Examiner contended that *Uenishi et al.* and *Kubo et al.* substantially teach the entire claimed structure except that the trenches formed in first and second directions, and that it would have been obvious to combine the teachings of *Blanchard* with either *Uenishi et al.* or *Kubo et al.* to arrive at Applicant's claims.

Claim 1 is submitted to be patentable over the prior art as discussed above. Combining the features of *Uenishi et al.* and *Kubo et al.* and of *Blanchard* of having trenches formed in first and second directions still does not meet Applicant's amended claim 1. Specifically, the combined structure as suggested does not have any opening for purpose of contacting different materials, and further without "said first conductive layer having conductivity higher than the conductivity of said conductive material," in which the conductive material is deposited inside the gate trench as recited in amended claim 1. Claims 2-12 and 14 are dependent claims dependent upon claim 1. Claims 2-12 and 12 include all the limitations of claim 1 in addition to their own limitations, are submitted to be, *a fortiori*, patentable.

As for claims 15-19 and 21-31, claims 15 and 27 are independent claims. Claims 16-19, 21-26 and 28-31 are dependent claims. Independent claims 15 and 27 are first highlighted for discussion.

To begin with, there is no suggestion in any of the cited references to combine the different features as suggested by the Examiner to arrive at Applicant's claims 15 and 27. To support the conclusion that the claimed invention is directed to obvious subject matter, either the reference must expressly or impliedly suggest the claim invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the reference. *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). Here, nowhere in cited references is their any mention of combining a trench structure having a first conductive layer contacting the conductive material in the trenches with another structure having the trenches formed in first and second directions. Applicant respectfully submits that the combination is based on a conclusory statement which can only be made from Applicant's disclosure. Relying on "common knowledge" in the art without evidentiary support in the record as the principal evidence upon which a rejection was based is inappropriate. *In re Zurko*, 258 F.3d 1379, 1385, 59 USPQ.2d 1693, 1697 (Fed. Cir. 2001).

Notwithstanding the lack of teaching and motivation to combine the references as mentioned above, in a manner similar to claim 1, to further distinguish over the prior art, claims 15 and 17 have been amended to include the additional recitation of "said first conducting layer having conductivity higher than the conductivity of said conductive material." The suggested combination does not have a first layer with higher conductivity than the conductive material in the trench gates. Accordingly, independent claims 15 and 27 as amended, are patentable over the prior art.

As for the remaining dependent claims 16-19, 21-26 and 28-31, they are directly or indirectly dependent on their respective independent claims. Specifically, claims 16-19 and 21-26 depend directly or indirectly on claim 15. Claims 28-31 depend directly or indirectly on claim 27. Each of the mentioned dependent claims includes limitations of its respective independent claim on the top of its own limitations, is thus submitted to be even more patentable. Patentability is dependent upon on the entire claimed combination, including those limitations found in independent claims 15 and 27.

For the above reasons, Applicant respectfully requests withdrawal of the rejection on Claims 1-12, 14-19 and 21-31, under 35 U.S.C. § 103(a).

In the aforementioned Office Action, claims 20 and 32 were objected to, but would be allowable if rewritten in independent form including all the limitations of the

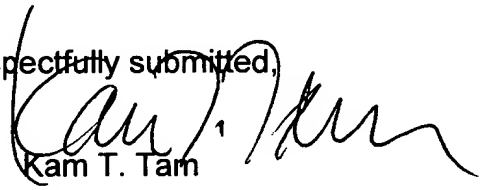
respective base claims 15 and 27 and any intervening claims.

By this amendment, claims 32 has been rewritten as an independent claim. Claim 20 has been canceled and replaced with new claim 33. Claims 32 and 33 are submitted to include all the limitations of the base claims 15 and 27, respectively, and with all the intervening claims.

The cited by non-applied references have been studied, but are submitted to be less relevant than the relied upon references.

In view of the foregoing, by this amendment, the application is believed to be in condition for allowance. Reconsideration and allowance are respectfully requested.

Respectfully submitted,



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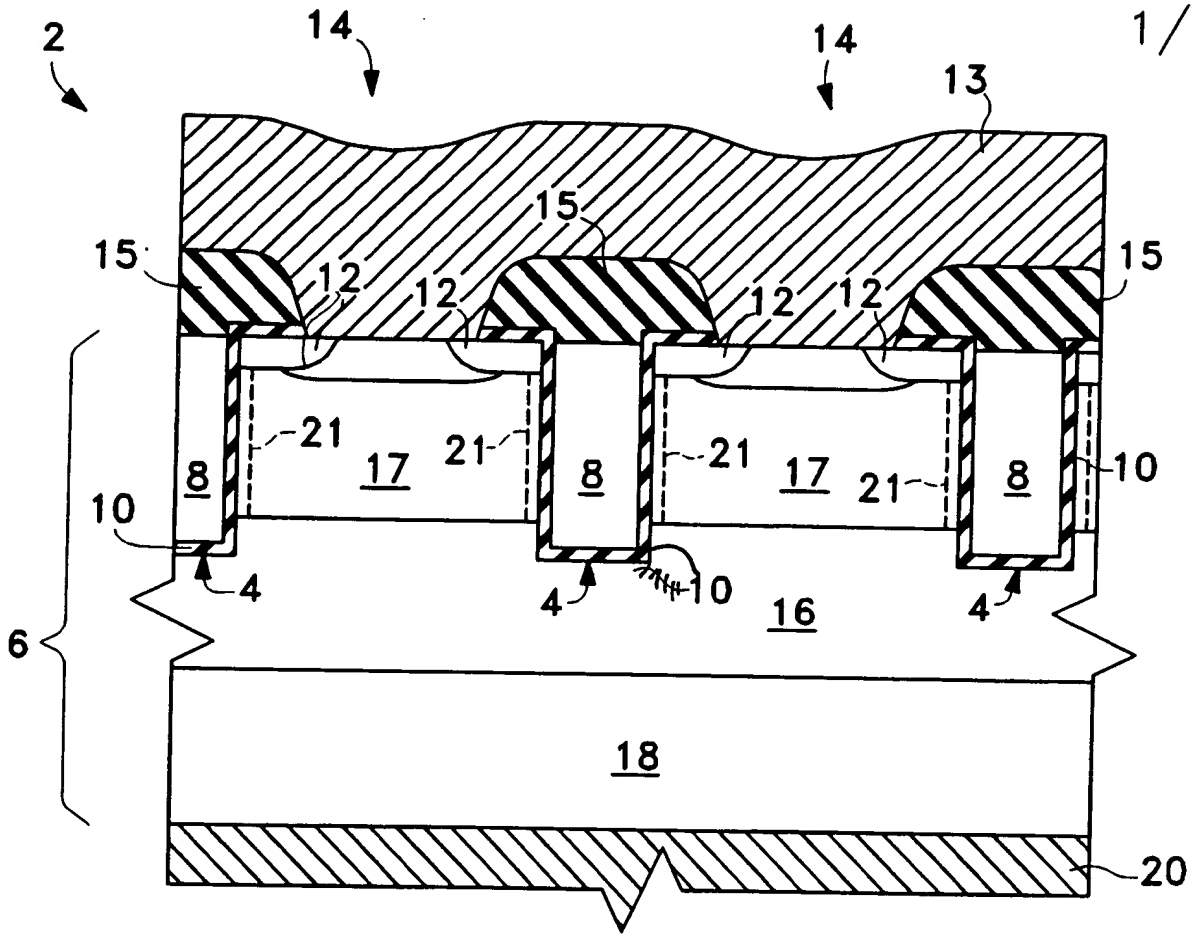

FIG. 1 (PRIOR ART)

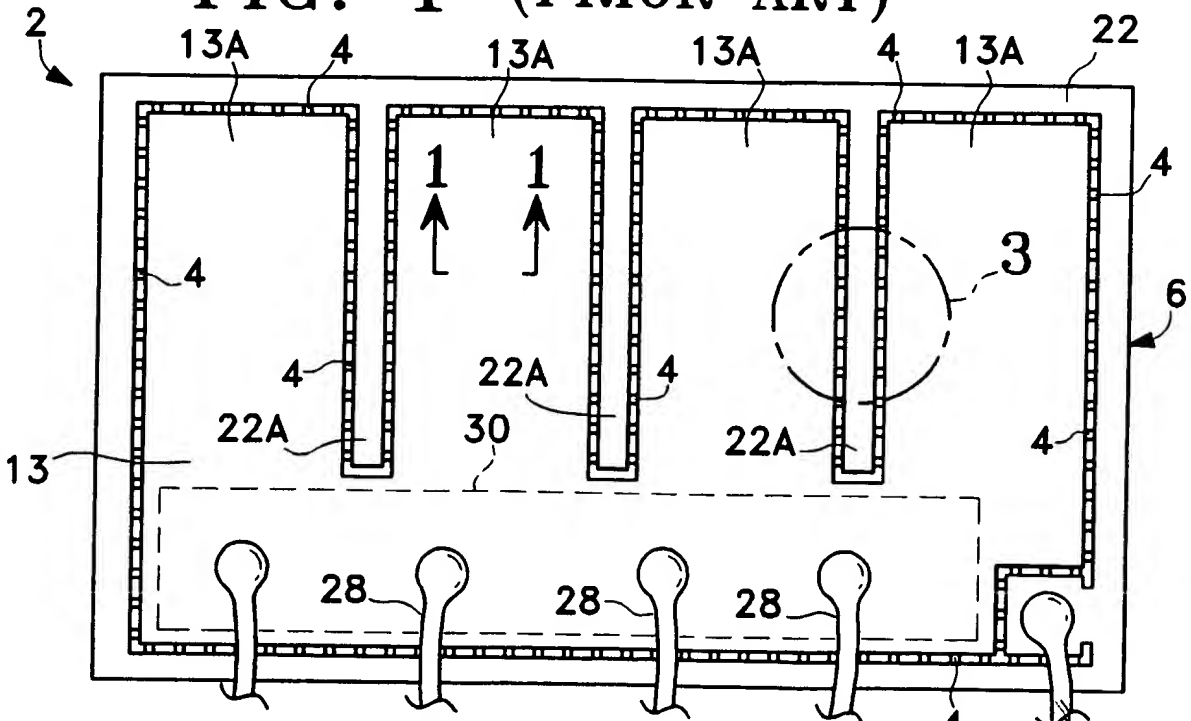

FIG. 2 (PRIOR ART)

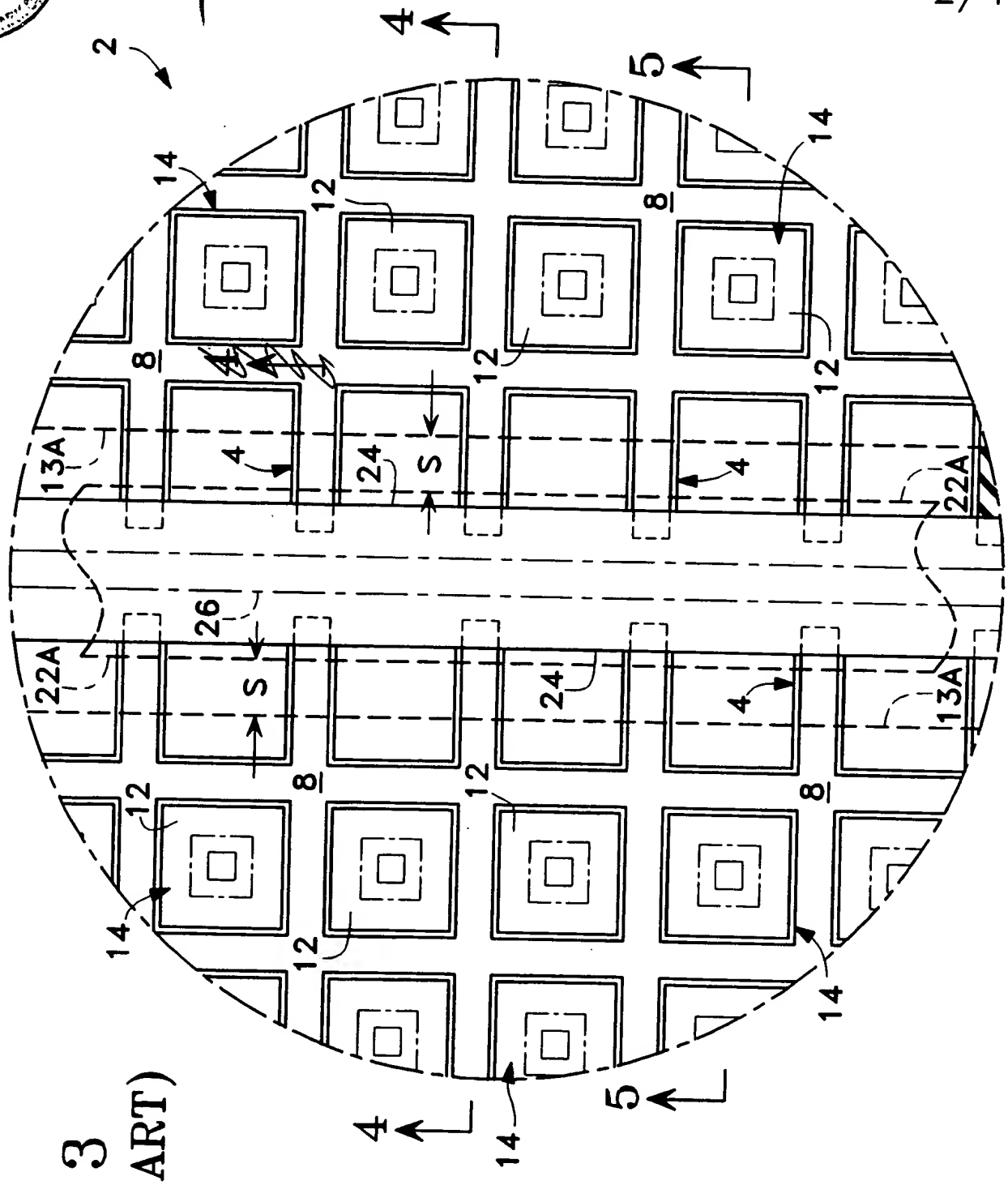

FIG. 3
(PRIOR ART)

SPECIFICATION WITH MARKINGS TO SHOW AMENDED CHANGES

Serial Number : 09/139,935

Filing Date : August 25, 1998

Gate Contacting Scheme of a Trench MOSFET Structure

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to microelectronic circuits, and more particularly, to electrical contacting schemes of trench gates in trench MOSFET (Metal Oxide Semiconductor Field Effect Transistor) devices.

Description of the Related Art

Power semiconductor devices have [long] been used as power switches [in] for various applications. Advent in semiconductor technolog[y]ies enable[s] these power devices to operate with high reliability and performance.

One type of power MOSFET (Metal Oxide Semiconductor Field Effect Transistor) device[s] that shows prominence in application is the trench[-]gate MOSFET power device. In a trench-gate MOSFET device, intersecting trenches which define a plurality of cells are formed in a silicon substrate. Fig. 1 is a cross-sectional view of part of a trench-gate MOSFET device signified by the reference numeral 2. There is a plurality of trenches 4 formed in a substrate 6. The trenches 4 are filled with conductive material 8 separated from the substrate 6 with a thin layer of insulating material 10. There is also a source layer 12 deposited in a body layer 17 which in turn is deposited in

the semiconductor substrate 6. The source layer 12 is in contact with a source metal layer 13. An insulating layer 15 separates the conductive material 8 from the source metal layer 13. As arranged, a plurality of MOSFET cells 14 [are] is formed in the substrate 6. Specifically, for each MOSFET cell 14, the source layer 12, the conductive material 8 and insulating material 10 constitute respectively the source, gate and gate oxide layer of a MOSFET. In addition, a lightly doped epitaxial layer 16 coupled with a heavily doped contact layer 18 attached to a drain metal layer 20 forms the common drain of the device 2.

Power MOSFET device with trench gates provide many advantages. To begin with, the channels, signified by the reference numeral 21 in Fig. 1, of the MOSFETs are arranged in a vertical manner, instead of horizontally as in most planar configurations. The consequential benefit is that a higher degree of integration on a semiconductor substrate can be realized. More importantly, since the channel direction is vertical, the lateral current paths are basically eliminated. As a result, the overall channel resistance is reduced. Reduction in channel resistance substantially curtails [the] Ohmic loss during the power-on state of the MOSFET, which in turn provides lower power consumption and further alleviates heat dissipation.

Advantageous as it appears for a trench-gate MOSFET structure, heretofore, there have been technical complications in providing electrical contacts to the conductive material 8 inside the trenches 4.

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Fig. 2 is a top plan view of an overall metallization scheme of a conventional power MOSFET structure, such as the structure 2 shown in Fig. 1. Fig. 1, as described above, is a cross-sectional view taken along the line 1-1 of Fig. 2. For clarity and conciseness in illustration, other metal layers such as the metal layers for the terminal circuits are not shown in Figs. 1 and 2. As can be seen in Fig. 2, the source metal layer 13 is deposited on the semiconductor substrate 6 with a plurality of protruding fingers 13A. In a similar manner, the gate metal 22 is also deposited on the semiconductor substrate 6 with a plurality of protruding fingers 22A . The protruding fingers 13A and 22A electrically separate but interleave with each other on the surface of the substrate 6 as shown in Fig. 2.

Fig. 3 is an enlarged view taken within the circle 3 of Fig. 2. Figs. 4 and 5 are cross-sectional views taken along the lines 4-4 and 5-5, respectively, of Fig. 3. Figs. 3-5 highlight the relationship of the source metal layer 13 and the gate metal layer 22 in more details. For clarity in illustration, the metal layers and contact openings are shown in ghost lines in Fig. 3.

As shown in Figs. 3-5, the source metal finger 13A is disposed in contact with the source layer 12. The gate metal finger 22A is disposed in contact with a poly runner 24 through a contact opening 26. The poly runner 24 is in turn deposited in contact with the conductive material 8 in the trenches 4.

There are several disadvantages associated with the

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metallization scheme of the conventional structure 2 as shown in Figs. 1-5. First, the gate metal fingers 22A coupled with the poly runner 24 and the associated contacting trenches 4 use up precious semiconductor spaces on the substrate 6, which spaces could have been used for active cells 14. Furthermore, the conductive material 8 in the trenches 4, even though heavily doped, does not assume [a] conductivity comparable to that of metal. Specifically, the material 8 in the trenches 4 with the relatively high resistivity manifests itself as distributed resistance along the gate-to-source input path, thereby undermining the [time] timing response of the structure 2. Phrased differently, the relatively low conductivity of the material 8 retards the RC (resistance-capacitance) time constant of the gate-to-source input path of the structure 2 and renders the structure 2 not suitable for use in high frequency applications.

It also should be emphasized that in the design of a power MOSFET, providing a lower power-on resistance R_{ON} is of paramount importance. The power-on resistance R_{ON} of a power MOSFET device is defined as the gross Ohmic resistance through the device during the power-on state. Lower power-on resistance R_{ON} not only curtails power consumption and thus cuts down wasteful heat dissipation, it also prevents the power MOSFET device from robbing away any intended driving voltage to the circuits that the MOSFET device drives. That is, lower Ohmic drop passing through the power MOSFET device during normal operation avails the target circuit driven by the MOSFET device with a less distorted driving voltage. Modern-day MOSFET power devices can now be made with power-

on resistance R_{ON} in the milliohm (mΩ) range. The segmented source metal 13 unnecessarily adds source metal resistance to the overall power-on resistance R_{ON} of the structure 2.

The fabrication of the conventional structure 2 also requires a relatively tight manufacturing control. For example, the metal-to-metal separation between the source metal layer 13 and the gate metal layer 22, identified in Figs. 3-5 as separation S, needs to be tightly controlled. Thus, if the separation S falls beyond a certain manufacturing tolerance, there is a risk of electrical shorts between the metal layers 13 and 22 and is detrimental to the production yield. To maintain the tolerance, constant monitoring is required during processing.

It also needs to be mentioned that the structure 2 does not have a relatively wide degree of flexibility during die-bonding. Reference is now directed [back] to Fig. 2. During the die-bonding process, the electrical terminals of the structure 2, such as the source metal 13, need to be connected to a chip carrier (not shown) via the bond wires 28. As shown in Fig. 2, the bond wires 28 for the source metal layer 13 is confined to an area designated by the reference numeral 30 which is away from the gate metal fingers 22A on the substrate 6. Any mistepping of the bond wire 28 beyond the confined area 30 may result in electrical shorts between the metal fingers 13A and 22A.

[Instruments and appliances] Electronic products are now built with ever increasing complexity providing various functions which require high frequency operations and

critically depend on the reliable supply of power by the power devices. There has [always] been a long-felt demand to provide dependable, responsive and robust power devices to these modern-day [instruments] products without the aforementioned shortfalls.

SUMMARY OF THE INVENTION

It is accordingly the object of the invention to provide a MOSFET structure with a low gate resistance thereby allowing the structure to be suitable for high-frequency applications.

It is another object of the invention to provide a MOSFET structure with a low power-on resistance.

It is yet another object of the invention to provide a MOSFET structure with high packing density.

It is still another object of the invention to provide a MOSFET structure with less stringent manufacturing tolerance control in the metal deposition process and further with flexibility in the wire-bonding process.

The MOSFET structure in accordance with the invention accomplishes the above objectives via a novel metal routing scheme. In [the] a preferred embodiment, the MOSFET structure of the invention includes criss[-]crossing trenches formed in a semiconductor substrate. The trenches include inner surfaces filled with conductive material which in turn is electrically separated from the substrate by insulating material. The conductive material is in contact

with an overlying first metal layer through a plurality of first contact openings formed in a first insulating layer which is sandwiched between the first metal layer and the trenches. The conductive material in the trenches and the first metal layer constitute the gate of the MOSFET structure. There is also a second metal layer in contact with a source layer formed in the substrate through a plurality of second contact openings formed in a second insulating layer which is sandwiched between the first metal layer and the second metal layer. The second metal layer and the source layer constitute the source of the MOSFET structure. In the MOSFET structure of the invention, the gate and source are connected through separate metal layers. As arranged, the gate and source of the MOSFET structure are connected through separate metal layers on the semiconductor substrate. Consequently, each metal layer maintains a higher conductivity and thus faster frequency response. The semiconductor structure formed in accordance with the invention can also assume a higher packing density with lower power-on resistance.

These and other features and advantages of the invention will be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings, in which like reference numerals refer to like parts.

DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional view of a conventional trench MOSFET array having a plurality of trenched cells;

Fig. 2 is a top plan view illustrating the overall

metallization scheme the conventional trench MOSFET array as shown in Fig. 1 which is taken along the line 1-1 of Fig. 2;

Fig. 3 is an enlarged view taken within the circle 3 of Fig. 2;

Fig. 4 is a cross-sectional view taken along the line 4-4 of Fig. 3;

Fig. 5 is a cross-sectional view taken along the line 5-5 of Fig. 3;

Fig. 6 is a top plan view illustrating the overall metallization scheme of the first embodiment of the invention;

Fig. 7 is an enlarged view taken within the circle [6] 7 of Fig. 6;

Fig. 8 is a cross-sectional view taken along the line 8-8 of Fig. 7;

Fig. 9 is a cross-sectional view taken along the line 9-9 of Fig. 7;

Fig. 10 is a cross-sectional view of another variation of the metallization scheme in accordance with the invention in which the source metal layer is plated with another metal layer;

Fig. 11 is a cross-sectional view of yet another variation of the metallization scheme in accordance with the invention in which the source metal layer is plated with another metal layer interposed with a primer layer;

Fig. 12 is a top plan view of a second embodiment of the invention comprising low-resistance and low-capacitance cells interleaving with each other formed in the silicon substrate;

Fig. 13 is a cross-sectional view taken along the line 13-13 of Fig. 12;

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Fig. 14 is a cross-sectional view taken along the line 14-14 of Fig. 12; and

Fig. 15 is another arrangement in accordance with the invention in which the cells are fabricated as elongated in shape.

DETAILED DESCRIPTION OF THE INVENTION

Reference is now made to Figs. 6-9 which show the first embodiment of the invention. The semiconductor structure of this embodiment is generally signified by the reference numeral 40. Fig. 5 is a top plan view of the structure 40 illustrated as packaged on a chip carrier 42. The relationship between the structure 40 and the chip carrier 42 in association with the bonding wires 86 will be explained later in this specification. The structure 40 includes a plurality of semiconductor cells 44 in which some of the cells 44 are shown in hidden lines in Fig. 6.

Fig. 7 is an enlarged view taken within the circle 7 of Fig. 6. For purpose of illustration, the overlying metal layers in Fig. 7 are removed. In additional, the contact openings are shown in ghost lines. However, the metal layers and the contact openings are clearly shown in Figs. 8 and 9 which are cross-sectional side views taken along the lines 8-8 and 9-9, respectively, of Fig. 6.

Reference is now directed to Figs. 6-9. The semiconductor structure 40 is formed on a semiconductor substrate 46 having a major surface 48. There is a plurality of intersecting trenches 50A and 50B formed in the substrate 46. Some trenches 50A are oriented in a first

direction, such as the horizontal direction 52 as shown in Fig. 7. Likewise, other trenches 50B are oriented in a second direction, such as the vertical direction 54 as also shown in Fig. 7. The trenches 50A and 50B are filled with conductive material 56 which is electrically separated from the substrate 46 with a thin layer of insulating material 58. The materials used for the conductive material 48 and the insulating material 50 can [be] respectively <u>be</u> polycrystalline silicon (Si) and silicon dioxide (SiO_2), for example. Disposed atop the trenches 50A and 50B is a first insulating layer 60 which is patterned with a plurality of contact openings, called the first contact openings 62 formed in the layer 60. Above the first insulating layer 60 is a first conductive layer 64 which is disposed in contact with the conductive material 56 in the trenches 50A and 50B through the first contact openings 62.

The first metal layer 64 in this embodiment is formed of criss[-]crossing segments running in the directions 52 and 54 and is disposed in alignment with the trenches 50A and 50B. For example, the segments of the first metal layer 64 shown in Fig. 8 are running in the second direction 54.

Over the first conductive layer 64 is a second insulating layer 66. A second conductive layer 68 is deposited above the second insulating layer 66. The second conductive layer 68 is disposed in contact with the semiconductor substrate 46 through another plurality of contact openings, called the second contact openings 70.

In this embodiment, the first and second conductive

layers 64 and 68 are made of aluminum (Al). The first and second insulating layers 60 and 66 are made of undoped silicon dioxide (SiO_2). However, other materials can be used as substitutes. For instance, material for the first and second conductive layers 64 and 68 can be copper (Cu), aluminum silicide (AlSi), or alloy of aluminum, silicon and copper (AlSiCu). The material for the first and second insulating layers 60 and 62 can be PSG (phosphorous silicon glass) BPGS (borophosphorous silicon glass), for example.

The intersecting trenches 50A and 50B define the plurality of MOSFET cells 44. Each MOSFET cell 44 includes a source layer 72 which in turn is deposited in a lightly doped body layer 74 (Fig. 8). The source layer 72 is disposed in contact with the second conductive layer 68 which is the source metal layer in this case. For each MOSFET cell 44, the source layer 72, the conductive material 56 and insulating material 58 constitute respectively the source, gate and gate oxide layer of a MOSFET cell. The body layer 74 is deposited in an epitaxially grown layer 76. The lightly doped epitaxial layer 76 coupled with a heavily doped contact layer 78 (Fig. 9) attached to a drain metal layer 80 (Fig. 9) form the common drain of the structure 40.

The MOSFET 40 in accordance with the invention can provide substantially improved performance both in the high-frequency and steady-state operations over most prior art counterparts, such as the structure 2 shown in Figs. 1-5. First, without the interleaving gate metal fingers, such as the gate metal fingers 22A coupled with the poly runner 24 as in the structure 2 shown in Figs. 2-5, all spaces are

almost fully utilized for the active cells 44 placement. That is, the architectural layout of the inventive structure 40 is different form most prior art structures, such as the structure 2 shown in Figs. 1-5, in which a substantial portion of the semiconductor space is dedicated for non-active cells. The structure 40 of the invention can thus achieve a high packing density.

The first conductive layer 64 above the trenches 50A and 50B is highly conductive. As a consequence, the resistance component of the RC time constant, which determines the time response of the gate-to-source input path as described above, is significantly reduced. This feature facilitates the turn-on and turn-off of the structure 40, thereby enabling the structure 40 to function responsively in high-frequency applications.

The second metal layer 68, the source metal layer in this case, is a substantially continuous layer and thus can maintain a high conductivity. The consequence benefit is that the continuous layer 68 contributes a lower power-on resistance R_{ON} of the structure 40. As mentioned before, modern-day power devices can achieve a power-on resistance R_{ON} in the milliohm (mΩ) range. The continuous second metal layer 68 makes a significant difference in maintaining a low power-on resistance R_{ON} within the sub-milliohm range.

With no interleaving metal fingers, such as the fingers 13A and 22A of the structure 2 shown in Figs. 2-4, side-by-side electrical shorts between the first metal layer 64 and the second metal layer 68 are less of a concern because the

two layers 64 and 68 are separated by the thick second insulating layer 66. Thus, the structure 40 can be fabricated with no side-by-side metal separation rule in the active cell areas.

There is also more bonding flexibility for the structure 40 during the die-bonding process. Reference is now returned to Fig. 6. The structure 40 is shown as disposed in the chip carrier 42 which is part of an eight-pin dual-in-line package in this example. The carrier 42 has a cavity 82 with a cavity bottom which is lined with a drain metal lead DML. During chip packaging, the drain metal layer 80 (Fig. 9) is directly soldered onto the drain metal lead DML, for example. The drain metal lead DML is electrically tied to the drain terminal pins D affixed externally on the carrier 42. The cavity 82 has a ledge portion 84 onto which the gate metal lead GML and the source metal leads SML are attached. Bond wires 86 are bonded between the leads GML and SML and the relevant metal layers of the structure 40. For example, the source metal lead SML is bonded to the second metal layer 68 through the bond wires 86. Similarly, the gate metal lead GML is bonded to a gate metal layer 69 through the bond wire 86. As can be seen in Fig. 6, there is more flexibility in placing the wires 86 on the second conductive layer 68 because it is continuous and thus provides a larger bondable area. That is, there is no need to restrict the bonding to a confined area, such as the area 30 for the structure 2 as shown in Fig. 2.

To further achieve a lower power-on resistance R_{ON}, the

second conductive layer 68 can be plated with a highly conductive metal layer 90. Fig. 10 shows such an arrangement in which a highly conductive metal such as copper (Cu) is electroplated onto the relatively thinly deposited second conductive layer 68 which is made of aluminum (Al). Aluminum has a better adhesiveness with silicon and silicon dioxide and thus the second conductive layer 68 which is made of aluminum is interposed between the plated layer 90 and the substrate 46.

If the plated layer 90 is made of material which has a lesser affinity with aluminum, a primer layer 92 can be sandwiched between the plated layer 90 and the second conductive layer 68 as shown in Fig. 11. For instance, the plated layer 90 and the primer layer can be made respectively of nickel (Ni) and tin (Sn), in which tin is "wettable" to both nickel and aluminum in the eutectic states.

Figs. 12-14 show a second embodiment of the invention generally signified by the reference numeral 94. Fig. 12 is a top plan view of the structure 94. Figs. 13 and 14 are cross-sectional views taken along the lines 13-13 and 14-14, respectively, of Fig. 12. The structural arrangement of this embodiment is substantially the same as the previous embodiment with the exception that there are two types of cells, namely, the low-resistance cells 44 and the low-capacitance cells 93 formed in the substrate 46. The low-resistance cells 44 are more or less similar to the cells 44 as described in the previous embodiment and is therefore not repeated in here. However, to facilitate description, the

trenches 50A and 50B are now called low-resistance trenches which are wider than the corresponding trenches 96A and 96B of the low-capacitance cells 93. Furthermore, the low-resistance trenches 50A and 50B are disposed in contact with the first conductive layer 64 as described previously. The characteristics of the low-capacitance cells 93 are herein described.

Each low-capacitance cell 93 includes a low-capacitance trench 96A or 96B which is narrower in width than the corresponding low-resistance trench 50A or 50B in each low-resistance cell 44. Thus the interior surface area, the area encompassing the conductive material 56, of each low-capacitance trench 96A or 96B is substantially reduced, resulting in lower parasitic capacitance associated with each trench 96A or 96B. Because of the narrower trench width, it may be difficult to form a contact opening, such as the first opening 66 above each low-resistance trench 50A or 50B, as shown in Fig. 3. Thus, the contact opening associated with the first metal layer above the low-capacitance trenches 96A and 96B are dispensed with. As a result, each low-capacitance cell 93 may carry a higher gate resistance R_G. However, the smaller trench interior surface area renders each trench 96A or 96B with much lower gate-to-drain C_{GD} capacitance.

To optimize the RC time constant of the structure 94 in high-frequency operations, the structure 94 can be laid out with certain number of rows of low-capacitance cells 93 interleaved with another certain number of rows of low-resistance cells 44 in the substrate 46, as shown in Figs.

12-14. Likewise, a certain number of columns of low-capacitance cells 93 can be interleaved with another number of columns of low-resistance cells 44 in the substrate 46, as shown in Figs. 12-14. As a further alternative, a combination of the above arrangements can also be formed in the substrate 46.

As with the previous embodiment, to further reduce the power-on resistance R_{ON}, the second conductive layer 68 can be plated with another highly conductive layer, in the similar manner as the layer 90 plated onto the layer 68 shown in Figs. 10 and 11. For clarity and conciseness in description, the plating of the second conductive layer 68 is not further [repeated] elaborated in here.

Finally, other changes are possible within the scope of the invention. The embodiments as described include rectangular or square cells 44 and 93. The cells can well assume other configurations or shapes such as triangular, hexagonal, or octagonal, to name just a few. By way of illustration, the cells can be elongated in shape. Fig. 15 shows such an arrangement in which the cells 98 are fabricated in the form of strips with corresponding elongated first and second openings 100 and 102. In addition, the gate metal ring layer 69 can be dispensed with, with only the gate metal pad 79 (Fig. 6) exposed for bonding. That is, the gate metal pad 79 can be directly electrically tied to the first metal layer 64, instead of passing through the gate metal ring layer 68 as intermediary. This arrangement can completely eliminate the need to monitor the side-by-side metal separation in the

actual cell area. Furthermore, in the first embodiment, there is a plurality of first contact openings 62. The purpose is to secure a firm contact surface on the conductive material 56. The areas above the conductive material 56 which the trenches 50A and 50B intersect may include concave dimples which may provide inferior contacts. As such, the contact openings 62 are preferably formed beyond the dimples. However, in sufficiently narrow trenches, such concave dimples may not exist. Should that be the case, the first contact openings 62 can be one continuous opening, instead of segmented as shown in Fig. 7. The device fabricated in accordance with the invention need not be a power MOSFET as described. It can well be slightly modified and used for other types of device, such as a dynamic random access memory (DRAM) cell, an insulated gate bipolar transistor (IGBT), or a charge-coupled-device (CCD), to name just a few. It will be understood by those skilled in the art that these and other changes in form and detail may be made therein without departing from the scope and spirit of the invention.

SPECIFICATION WITH MARKINGS TO SHOW AMENDED CHANGES

ABSTRACT

A trench MOSFET (Metal Oxide Semiconductor Field Effect Transistor) structure includes criss[-]crossing trenches formed in a semiconductor substrate. The trenches include inner surfaces filled with conductive material which [in turn] is electrically separated from the substrate by insulating material. The conductive material is in contact with an overlying first metal layer through a plurality of first contact openings formed in a first insulating layer which is sandwiched between the first metal layer and the trenches. The conductive material in the trenches and the first metal layer constitute the gate of the MOSFET structure. There is also a second metal layer in contact with a source layer formed in the substrate through a plurality of second contact openings formed in a second insulating layer which is sandwiched between the first metal layer and the second metal layer. The second metal layer and the source layer constitute the source of the MOSFET structure. As arranged, the gate and source of the MOSFET structure are connected through separate metal layers on the semiconduct[ive]or substrate. [As a consequence] Consequently, each metal layer maintains [a] higher conductivity and thus faster frequency response. The semiconductor structure formed in accordance with the invention can also assume a higher packing density with lower power-on resistance.

SPECIFICATION WITH MARKINGS TO SHOW AMENDED CHANGES